REMARKS/ARGUMENTS

In the Office action dated March 29, 2006, claims 1-22 were rejected. Claims 1-22 have been resubmitted. Claims 14 and 22 have been amended. New Claim 23 has been added. The amendments to the claims were not made to avoid the cited references. Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

Claim Rejections

Claims 1-6, 8-11, 13-18, and 20-22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley (U.S. Pat. No. 6,215,876), in view of Pozidis (U.S. PG-Pub. No. 20030005383), and further in view of Johnson et al. (U.S. Pat. No. 6,587,804). Claims 7, 12, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al., and further in view of Yoshimura (U.S. Pat. No. 5,123,020).

Gilley (U.S. 6,215,876)

Gilley teaches evaluation of *the number of errors* in a received cryptographic initialization vector (IV) to determine, on the basis of statistical probability, whether an anticipated initialization vector has bit errors caused by channel impairment (i.e., resulting in a small number of errors (=/< 4/64 bits)), or an incorrect prediction due to prior acceptance of an erroneous IV (i.e., resulting in a large number of errors (e.g., about 32/64 bits)). Gilley further teaches, in the preferred embodiment, coasting in the presence of bit errors in the received IV, i.e., ignoring such bit errors.

Claim 1

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al.

Claim 1 recites in part: "A bit error detection circuit comprising: ... *a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.*"

Applicant would like to point out that "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness." (MPEP 2142). As is readily apparent from the below, *prima facie* obviousness has not been established in this case.

Teaching Away by Gilley

In stark contrast to Applicant's claim 1, Gilley teaches *ignoring* or coasting by the received IV *in the presence of bit errors*. For example, Gilley states (col. 5, lines 20-28):

"Coasting systems ... (a) predict the correct IV, (b) detect if the received IV does not match the predicted IV and, further, (c) if so, ignore or coast by the received IV .... The preferred embodiment therefore utilizes ... coasting ... in the presence of bit errors to transmitted IV caused by the communications channel ... ."

Thus, Gilley, which teaches ignoring bit errors, clearly teaches away from Applicant's claim 1, which recites *a correction circuit* that *corrects any error* in the actual next bit to provide a *corrected* actual next bit. Teaching away from the claimed invention by a reference is a *per se* demonstration of lack of *prima facie* obviousness.

Accordingly, claim 1 defines an invention which is unobvious over Gilley, Pozidis, and Johnson, taken singularly or in combination.

Improper Combining of References with Gilley

The Office action states that "It would have been obvious to one of ordinary skill in the art ... to use a correction circuit to correct the bits in Gilley's

invention, since one of ordinary skill in the art would have realized that enabling Gilley's invention to correct bits would have made the invention [of Gilley] more beneficial ... ." Applicant does not concur for the following reasons.

The invention of Gilley relies on evaluation of *the number of errors* in a received initialization vector (see, for example, col. 6 line 36 – col. 7, line 8, and Fig. 4 of Gilley). Therefore, *correction* of errors (in the received initialization vector) would *disable* Gilley's invention. Modification of the teaching of Gilley as suggested in the Office action, for example by combining Gilley with the teaching of Podizis to include a correction circuit, would *destroy the intent, purpose, and functionality* of the Gilley reference. Thus, a suggestion to combine Gilley with Pozidis is improper, and a *prima facie* case of obviousness on the basis of Gilley combined with Pozidis cannot be properly made. (See, MPEP 2143.01: The Proposed Modification Cannot Change the Principle of Operation of A Reference. *In Re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959); and The Proposed Modification Cannot Render the Prior Art Unsatisfactory for its Intended Purpose. *In Re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).)

For the reasons cited above, Applicant submits that claim 1 defines an invention which is unobvious over Gilley, Pozidis, and Johnson, taken singularly or in combination.

Claims 2-7

Claims 2-6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al. Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al., and further in view of Yoshimura (U.S. Pat. No. 5,587,804).

Claims 2-7 depend directly on indirectly from claim 1. Therefore, each of claims 2-7 defines an invention which is patentable over the cited references for at least those reasons given above with respect to claim 1.

Claim 8

Claim 8 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al.

Claim 8 recites in part: "A bit error detection circuit comprising: ... a third logic element that receives the output signal and *corrects* the actual (N+1)-th bit ... ."

The above remarks regarding claim 1 are similarly applicable to claim 8. Thus, in contrast to Applicant's claim 8, Gilley teaches *ignoring* bit errors, i.e., Gilley clearly teaches away from Applicant's claim 8. Furthermore, as noted above, modification of Gilley for the *correction* of errors (in the received initialization vector) would *disable* Gilley's invention. Therefore, combining Gilley with Pozidis is improper, and a *prima facie* case of obviousness cannot be made on the basis of the cited references (see, MPEP 2143.01).

Accordingly, Applicant submits that claim 8 defines an invention which is unobvious over Gilley, Pozidis, and Johnson, taken singularly or in combination.

Claims 9-13

Claims 9-11 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al. Claim 12 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al., and further in view of Yoshimura.

Claims 9-13 depend directly on indirectly from claim 8. Therefore, each of claims 9-13 defines an invention which is patentable over the cited references for at least those reasons given above with respect to claim 8.

Claim 14

Claim 14 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al.

Claim 14 recites a method comprising "... providing an error signal and *correcting the actual next bit*."

The above remarks regarding claim 1 and claim 8 are similarly applicable to claim 14. For example, in contrast to Applicant's claim 14, Gilley teaches *ignoring* bit errors, i.e., Gilley teaches away from the claimed invention. Furthermore, as noted above, the *correction* of errors (in the received initialization vector of Gilley) would destroy the intent, purpose, and functionality of Gilley's invention. Therefore, a *prima facie* case of obviousness cannot be made on the basis of the cited references (MPEP 2143.01).

Accordingly, Applicant submits that claim 14 defines an invention which is unobvious over Gilley, Pozidis, and Johnson, taken singularly or in combination.

Claims 15-20

Claims 15-18 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al. Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al., and further in view of Yoshimura.

Claims 15-20 depend directly on indirectly from claim 14. Therefore, each of claims 15-20 defines an invention which is patentable over the cited references for at least those reasons given above with respect to claim 14.

Claim 21

Claim 21 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al.

Claim 21 recites in part "A bit error detector comprising: ... a *corrector* coupled to the error signal output and having a *corrected actual next bit output*."

The above remarks regarding claim 1 are similarly applicable to claim 21. For example, Gilley teaches *ignoring* bit errors, i.e., Gilley clearly teaches away from Applicant's claim 21. Furthermore, as noted hereinabove, modification of Gilley for the *correction* of errors (in the received initialization vector) would *disable* Gilley's invention. Therefore, combining Gilley with Pozidis is improper, and a *prima facie* case of obviousness cannot be made on the basis of the cited references (MPEP 2143.01).

Accordingly, Applicant submits that claim 21 defines an invention which is unobvious over Gilley, Pozidis, and Johnson, taken singularly or in combination.

Claim 22

Claim 22 was rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson et al.

Claim 22 depends directly from claim 21. Therefore, claim 22 defines an invention which is patentable over the cited references for at least those reasons given above with respect to claim 21.

New Claim 23

New claim 23 recites in part: "A high-speed communications system, comprising: ... a pseudo-random bit sequence error detector, in signal communication with the communications channel, for detecting and *correcting any error in an actual next bit* of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises: ... *a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.*"

As noted above, Gilley teaches *ignoring* bit errors; therefore, Gilley teaches away from Applicant's new claim 23. Furthermore, as noted hereinabove, modification of Gilley for the *correction* of errors would *disable* Gilley's invention.

Accordingly, the cited references fail to teach or suggest the specific combination recited in new claim 23.

Support for Amendment to Claims

Support for the amendment to claim 14 can be found, for example, at original claim 14.

Support for the amendment to claim 22 can be found, for example, at original claims 21 and 22.

Support for New Claim 23

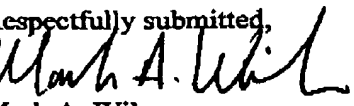
Support for new claim 23 can be found, for example, at paragraphs [0036], [0043], and [0048] of the specification, and Figures 1 and 4.

CONCLUSION

In light of the above, applicant submits that the claims are now in condition for allowance. Reconsideration and withdrawal of the Office action with respect to claims 1-22 is respectfully requested. Allowance of claims 1-23 is earnestly solicited.

In the event that the examiner wishes to discuss any aspect of this response, please contact the attorney at the telephone number identified below.

Respectfully submitted,



Date: June 28, 2006

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